Claims

What is claimed is:

1. A data processing system comprising:

(a) a bus coupling components in the data processing system;

(b) an external memory coupled to the bus;

(c) a programmable microprocessor coupled to the bus and capable of operation independent of another host processor, the microprocessor comprising:

a virtual memory addressing unit;

an instruction path and a data path;

an external interface operable to receive data from an external source and communicate the received data over the data path;

a cache operable to retain data communicated between the external interface and the data path;

at least one register file configurable to receive and store data from the data path and to communicate the stored data to the data path; and

a multi-precision execution unit coupled to the data path, the multi-precision execution unit configurable to dynamically partition data received from the data path to account for an elemental width of the data wherein the elemental width of the data is equal to or narrower than the data path, the multi-precision execution unit being capable of performing group floating-point operations on multiple operands in partitioned fields of operand registers and returning catenated results.

2. The data processing system of claim 1 wherein the multi-precision execution unit is capable of performing group add, group subtract and group multiply arithmetic operations on catenated floating-point data and, for each such group operation, returning catenated results of the operation to a register.

3. The data processing system of claim 1 wherein at least some of the group add, group subtract and group multiply arithmetic operations perform arithmetic operations on floating-point data stored in first and second operand registers and return the catenated result to a result register.

4. The data processing system of claim 3 wherein the result register is a different register than either the first or second operand registers.

5. The data processing system of claim 1 wherein the multi-precision execution unit is capable of executing a first plurality of group floating-point operations on floating-point data of a first precision and a second plurality of group floating-point operations on floating-point data of a second precision that is a higher precision than the first precision and wherein a number of data elements stored in partitioned fields of the operand registers for the first and second plurality of group floating-point operations is inversely related to the precision of the data elements.

6. The data processing system of claim 1 wherein the multi-precision execution unit is capable of executing group floating point operations that operate on 32-bit data elements and group floating-point operations that operate on 64-bit data elements and wherein a number of data elements stored in partitioned fields of operand registers used for the operations that operate

on 32-bit data elements is twice as many as a number of data elements stored in partitioned fields of operand registers used for the operations that operate on 64-bit data elements.

7. The data processing system of claim 1 wherein, when performing at least some of the group floating-point operations, the multi-precision execution unit operates on partitioned fields of operand registers in parallel and returns the catenated results to a register.

8. The data processing system of claim 1 wherein the multi-precision execution unit is capable of executing a plurality of group floating-point operations on floating-point data of a first precision and a plurality of group floating-point operations on floating-point data of a second precision that is a higher precision than the first precision and wherein, when performing at least one of the group floating-point operations on floating-point data of the first precision, the multi-precision execution unit operates on at least two partitioned operands in parallel.

9. The data processing system of claim 1 wherein the multi-precision execution unit is capable of performing group floating-point operations on catenated data having a total aggregate width of 128 bits.

10. The data processing system of claim 1 wherein the multi-precision execution unit is capable of performing group floating-point operations on floating-point data of more than one precision.

11. The data processing system of claim 1 wherein the multi-precision execution unit is capable of performing group integer operations on multiple operands in partitioned fields of operand registers and returning catenated results to a register.

12. The data processing system of claim 11 wherein the multi-precision execution unit is capable of performing group add, group subtract and group multiply arithmetic operations on catenated integer data and, for each such group operation, returning catenated results of the operation to a register.

13. The data processing system of claim 12 wherein at least some of the group add, group subtract and group multiply arithmetic operations perform arithmetic operations on integer data stored in first and second operand registers and return the catenated result to a result register.

14. The data processing system of claim 11 wherein the multi-precision execution unit is capable of executing a first plurality of group integer operations on integer data of a first precision and a second plurality of group integer operations on integer data of a second precision that is a higher precision than the first precision and wherein a number of data elements stored in partitioned fields of the operand registers for the first and second plurality of group integer operations is inversely related to the precision of the data elements.

15. The data processing system of claim 11 wherein, when performing at least some of the group integer operations, the multi-precision execution unit operates on partitioned fields of operand registers in parallel and returns the catenated results to a register.

16. The data processing system of claim 11 wherein the multi-precision execution unit is capable of executing a plurality of group integer operations on integer data of a first precision and a plurality of group integer operations on integer data of a second precision that is a higher precision than the first precision and wherein, when performing at least one of the group

integer operations on integer data of the first precision, the multi-precision execution unit operates on at least two partitioned operands in parallel.

17. The data processing system of claim 1 wherein the multi-precision execution unit is capable of performing one or more group data handling operations that operate on multiple operands in partitioned fields of one or more operand registers and returning catenated results to a register.

18. The data processing system of claim 17 wherein the one or more group data handling operations comprises a first group operation that converts a plurality of n-bit data elements in a first operand register and a plurality of n-bit data elements in a second operand register into a plurality of n/2-bit data elements in a result register.

19. The data processing system of claim 18 wherein the first group operation shifts each of the plurality of n/2-bit data elements by a specified number of bits during the conversion.

20. The data processing system of claim 17 wherein the one or more group data handling operations comprises a second group operation that interleaves a plurality of data elements selected from a first operand register with a plurality of data elements selected from a second operand register and catenates the data elements into a result register.

21. The data processing system of claim 17 wherein the one or more data handling operations comprises a group shift left operation that shifts bits of individual data elements catenated in an operand register to the left and clears empty low order bits of the individual data elements to zero.

22. The data processing system of claim 17 wherein the one or more data handling operations comprises a group shift right operation that shifts bits of individual data elements catenated in an operand register to the right and fills empty high order bits of the individual data elements with a value equal to a value stored in a sign bit of the individual data element.

23. The data processing system of claim 17 wherein the one or more data handling operations comprises a group shift right operation that shifts bits of individual data elements catenated in an operand register to the right and clears empty high order bits of the individual data elements to zero.

24. The data processing system of claim 17 wherein the multi-precision execution unit is capable of executing a first plurality of group data handling operations on data of a first precision and a second plurality of group data handling operations on data of a second precision that is a higher precision than the first precision and wherein a number of data elements stored in partitioned fields of the operand registers for the first and second plurality of group data handling operations is inversely related to the precision of the data elements.

25. The data processing system of claim 17 wherein, when performing at least some of the group data handling operations, the multi-precision execution unit operates on partitioned fields of operand registers in parallel and returns the catenated results to a register.

26. The data processing system of claim 17 wherein the multi-precision execution unit is capable of executing a plurality of group data handling operations on data of a first precision and a plurality of data handling operations on data of a second precision that is a higher precision than the first precision and wherein, when performing at least one of the group data

handling operations on data of the first precision, the multi-precision execution unit operates on at least two partitioned operands in parallel.

27. The data processing system of claim 1 wherein the multi-precision execution unit comprises a plurality of functional units.

28. The data processing system of claim 1 wherein the at least one register file comprises a plurality of registers that can be used to store operands and results for the group floating-point operations.

29. The data processing system of claim 1 wherein the multi-precision execution unit returns the catenated results to a register.

30. The data processing system of claim 1 wherein the at least one register file comprises a plurality of general purpose registers that can be used as operand and result registers for group floating-point operations.